

B.) Amendments to the Specification

[0049] An extended protocol processor architecture 50 consistent with the present invention is shown in Figure 3. Multiple ingress processors 52 and egress processors 54 can be provided as part of the architecture 50 to support aggregation of network data traffic from multiple LANs through a single gateway device. This also allows the ingress and egress processors 52, 54 to extend the functionality of the architecture 50 to include data compression, network data traffic switching and routing, and other compute intensive packet processing operations on a single gateway device implementing the architecture 50. Multiple switch fabrics 56 can also be incorporated into the architecture 50 to provide connection redundancy and increase the effective bandwidth of the switch fabric 56 through added connection parallelism. Multiple scalable arrays of data packet processors 58 can be directly connected to the switch fabrics 56 to provide various forms of protocol data processing, characterized as involving significant computation intensive operations. The individual data packet processors 58 may be configured to perform a single protocol conversion operation or, by selection, any of multiple related operations. For example, packet data can be compressed before encryption and decompressed following decryption. Single data processors 58 can be used to perform multiple compute intensive operations or the fast path processing of network data packets may be extended to include the transfer of data packets between multiple data packet processors 58 before finally being forwarded on to an egress processor 54. Thus, separate data compression/decompression and encryption/decryption data processors can be employed for reasons of architectural flexibility and simplicity. Multiple control processors 60 can also be included for both redundancy and increased capacity for handling control process flows and protocol negotiations.